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APPARATUS FOR MODELING IC SUBSTRATE NOISE UTILIZING IMPROVED DOPING PROFILE ACCESS KEY

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BACKGROUND OF THE INVENTION

16 1. Field of the Invention

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18 The present invention relates to substrate modeling. More particularly, the
19 present invention relates to modeling characteristics of a substrate using doping
20 profiles.

21 2. Description of the Related Art

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23 Integrated circuits are typically modeled, or simulated, prior to fabrication.
24 These simulation tools may be used to optimize performance of integrated circuits as
25 well as reduce the likelihood of failure of such circuits after fabrication. Thus,
26 simulation is advantageous since circuits may be easily redesigned without
27 duplicative fabrication costs.

28 Simulation tools are typically used to model the behavior of transistor devices
29 that are formed on a substrate as well as interconnect lines that connect these devices.
30 However, through the use of such tools, only a portion of the substrate is modeled.
31 By way of example, during simulation of a transistor device formed on a substrate
32 approximately 400 microns thick, a thickness of approximately 0.1 microns is
33 typically modeled. Since net doping levels vary throughout the substrate, modeling
34 only a fraction of the substrate yields an inaccurate simulation of the substrate
35 characteristics. Accordingly, it would be desirable if the entire depth of the substrate
36 were modeled.

5 Further, a substrate is not an ideal medium. Since recently developed
6 fabrication processes permit device feature sizes to be reduced, the frequency of
7 operation for transistor devices has increased with these developments. Similarly,
8 with such a reduction in device feature size, the distance between transistor devices
9 may be reduced. Since noise attenuates with the distance between the source of the
10 noise (e.g., power supply) and the receiver of the noise, this parasitic noise may easily
11 propagate to multiple devices. As a result, this parasitic noise may prevent these
12 transistor devices from operating correctly. More particularly, these negative
13 consequences may be considerable for sensitive semiconductor devices such as MOS
14 transistors. Thus, it would be desirable if substrate modeling could be performed to
15 detect this noise.

16 Noise may be transferred to the substrate by a circuit formed on the surface of
17 the substrate. This noise transfer may occur at various interfaces between the circuit
18 and the substrate. A circuit typically includes numerous devices connected by
19 conductive interconnect lines. Capacitance as well as resistance between the substrate
20 and an overlying interconnect line or device may create undesirable parasitic effects.
21 As a result, this parasitic noise may be transferred through the substrate to other
22 devices in the circuit. Thus, it would be desirable to model the interface between the
23 substrate and the circuit.

24 IC substrates, as well as portions of the substrates, are typically doped. By
25 way of example, portions of substrates may be doped to create device elements, such
26 as source and drain diffusion regions. Thus, substrates commonly include multiple
27 layers that contain various net doping levels. In addition, the resistance present in the
28 substrate varies with these net doping levels. These varied resistances affect the
29 current flow throughout the substrate and therefore the performance of integrated
30 circuits formed on the substrate. Thus, it would be desirable if these doping levels
31 could be considered during the substrate modeling.

32 In view of the above, it would be desirable if a system and method for
33 modeling substrate noise through varying doping levels were developed. In this
34 manner, noise flowing through the substrate as well as between the substrate and
35 devices formed on the substrate, may be modeled and eliminated. Accordingly, a

5 circuit may be designed to eliminate or reduce this noise at the design phase without
6 estimation or fabrication of the circuit.

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6 An invention is described herein which provides methods and apparatus for
7 modeling noise present in an integrated circuit substrate. This is accomplished by
8 obtaining a doping profile associated with the integrated circuit substrate. Through
9 vertically discretizing the doping profile, the doping profile is divided into a finite
10 number of discrete portions. Moreover, all doping profiles associated with the
11 integrated circuit substrate may be obtained and vertically discretized. The integrated
12 circuit substrate can then be modeled using one or more vertically discretized doping
13 profiles. In this manner, speed and accuracy may be balanced during the modeling
14 process.

15 According to one aspect of the invention, an integrated circuit substrate is
16 modeled by using an associated doping profile. A position on a surface of the
17 integrated circuit substrate is obtained. A combination of layers associated with the
18 position and defining a vertical column beneath the position is obtained. A doping
19 profile associated with the combination of layers is obtained. The doping profile
20 includes a plurality of portions, each of which is associated with a different range of
21 substrate depth. A model of the substrate may then be generated using the obtained
22 doping profile. Such modeling may similarly be performed using a set of doping
23 profiles.

24 According to another aspect of the invention, methods and apparatus for
25 characterizing an integrated circuit substrate are disclosed. A set of one or more
26 substrate doping profiles including a net doping level for each one of a plurality of
27 depths within an integrated circuit substrate is obtained. A set (e.g., combination) of
28 layers associated with the set of one or more substrate doping profiles is determined.
29 The set of layers is in an order in relation to a surface of the integrated circuit
30 substrate. By way of example, the set of layers may be sorted with respect to the
31 sequence in which the layers are used during the fabrication process of an integrated
32 circuit. The set of one or more substrate doping profiles is vertically discretized to
33 form a vertically discretized substrate doping profile. A specific combination of
34 layers is then associated with each vertically discretized substrate doping profile.

5 To simplify the number of computations required to model a high component
6 count substrate, there is included an improved technique for performing surface
7 gridding, which allows highly dense regions to be modeled with dense divisions while
8 less populated regions to be modeled with larger surface divisions. As an object is
9 introduced into the substrate, the local partition impacted is examined to determine if
10 additional divisions are needed for proper surface modeling. As an object is removed,
11 the local/global partitions impacted are reviewed to determine whether simplification
12 may be performed.

13 In another embodiment, the invention relates to a method for extracting the
14 capacitance value associated with a PN junction along the well-substrate interface for
15 use in modeling the substrate. The method includes receiving the 2-D or 1-D mesh
16 doping profile. The method includes finding a junction curve or transition region that
17 represents the transition between the well and the substrate bulk. The method further
18 includes finding a set of parameters α , β and γ to characterize the junction at a point
19 or a vertical discretization along the transition. During modeling, the set of
20 parameters α , β and γ is then employed, along with the input bias voltage value, to
21 calculate the thickness of the depletion region, which is in turn employed to calculate
22 the capacitance for the well-substrate junction at that point or vertical discretization.
23 The capacitance calculated is then employed to more accurately model the junction at
24 that point or vertical discretization, which leads to a more accurate model for the
25 substrate.

26 In yet another embodiment, the invention relates to a method for modeling a
27 substrate, which includes obtaining vertically discretized doping profiles in the
28 substrate to facilitate modeling. The method includes employing substrate region
29 names and substrate cross-section names as access keys to permit accessing of the
30 doping profiles. The use of the combination of region names and substrate cross-
31 section names as unique access keys simplifies access to doping profile information
32 for modeling purposes and yields valuable information pertaining to the presence of
33 p-type to n-type material transitions. The information pertaining to transitions may be
34 employed to improve substrate modeling accuracy through the inclusion of junction
35 capacitances with the modeling process.

BRIEF DESCRIPTION OF THE DRAWINGS

6 The present invention will be readily understood by the following detailed
7 description in conjunction with the accompanying drawings, wherein like reference
8 numerals designate like structural elements, and in which:

9 FIG. 1 is a surface view of an integrated circuit substrate in which the present
10 invention may be implemented.

11 FIG. 2A is a cross-sectional view along the line a-a' of FIG. 1.

12 FIG. 2B is an exploded view of FIG. 2A exhibiting levels of modeling that
13 may be used to simulate the structure illustrated in FIG. 1.

14 FIG. 3 is a layout view of each layer within FIG. 1 used to mask etching and
15 implantation during the fabrication process.

16 FIG. 4 is a graph illustrating an exemplary doping profile taken along the line
17 b-b' of FIG. 2A according to one embodiment of the invention.

18 FIG. 5 is a graph illustrating an exemplary doping profile taken along the line
19 c-c' of FIG. 2A according to one embodiment of the invention.

20 FIG. 6A is a flow diagram illustrating a method for characterizing a particular
21 technology which may be used in a circuit layout according to one embodiment of the
22 invention.

23 FIG. 6B is a diagram illustrating one method for obtaining a binary key to a
24 doping profile as provided in FIG. 6A.

25 FIG. 7 is a flow diagram illustrating a method for applying the characterized
26 technology obtained in FIG. 6A to a specific circuit layout according to one
27 embodiment of the invention.

28 FIG. 8A is an exemplary graph superimposing multiple doping profiles which
29 may be present in a substrate such as that illustrated in FIG. 2A.

30 FIG. 8B is an exemplary graph illustrating the absolute values of the slopes of
31 the resistivity associated with the doping profiles of FIG. 8A.

5 FIG. 8C is an exemplary graph illustrating the sum of the curves illustrated in
6 FIG. 8B.

7 FIG. 8D is an exemplary graph illustrating the integral of the summed curve
8 illustrated in FIG. 8C.

9 FIG. 9 is an exemplary block diagram illustrating the method for using a
10 doping profile to aid in the modeling process of FIG. 7 according to one embodiment.

11 FIG. 10 is an exemplary diagram illustrating a method for determining
12 resistances using a doping profile according to an embodiment of the invention.

13 FIG. 11A is an exemplary diagram illustrating a global grid provided across a
14 surface of the integrated circuit substrate according to an embodiment of the
15 invention.

16 FIG. 11B is an exemplary diagram illustrating over-gridding that splits a
17 segment of the global grid according to an embodiment of the invention.

18 FIG. 11C is an exemplary diagram illustrating local gridding used to refine the
19 horizontal discretization around devices and interconnect interfaces with the substrate.

20 To facilitate further understanding of this aspect of the present invention, Figs.
21 12A-12F depict a substrate and the partitioning process that occurs when two objects
22 are inserted in sequence.

23 Figs. 13 and 14 show, in one embodiment, the steps taken in initializing a
24 substrate and implementing the inventive surface gridding scheme while inserting an
25 object.

26 Fig. 15 illustrates, in accordance with one embodiment of the present
27 invention, the steps employed in removing an object from the substrate (step 1310 of
28 Fig. 13).

29 To facilitate further understanding of this aspect of the present invention, Figs.
30 16A-16D depict a substrate and the simplification process that occurs when an object
31 is removed.

5 Fig. 17 shows, in accordance with one embodiment of the present invention, a
6 technique for computing the three parameters α , β and γ from the input 2-D mesh
7 doping profile.

8 Fig. 18 shows a 2-D input mesh doping profile wherein the concentration of
9 impurities is known in each point of the triangles that comprise the mesh.

10 Fig. 19 illustrates, in one embodiment, an extrapolation coupled with binary-
11 search algorithm is employed to find the junction curve from the input 2-D mesh
12 doping profile.

13 Fig. 20 shows three perpendicular lines for three points on the junction curve
14 along which the widths of the depletion regions are determined.

15 Fig. 21 shows the division of the net doping profile $N_D-N_A(x)$ into q
16 subdivisions in the well part and n subdivisions in the substrate part.

17 Fig. 22 shows, in one embodiment, the algorithm that corresponds to the
18 search of X_p and Y_N for each voltage.

19 Figs. 23, 24, and 25 illustrate the function $F(Y)$ for different bias voltages V_{NP}
20 (0V, 0.25V, and 0.5V respectively) for one example.

21 Fig. 26 is a table showing the resultant widths of the depletion region for
22 various bias voltages of one example.

23 Fig. 27 is another table showing the resultant widths of the depletion region
24 for various bias voltages of one example.

25 Fig. 28 depicts an exemplary plot of voltages v_i versus the corresponding
26 widths (f_i).

27 Figs. 29, 30, 31, and 32 show exemplary results of the method for calculating
28 the three parameters α , β and γ in accordance with one embodiment of the present
29 invention.

30 Fig. 33 illustrates, in one embodiment, the steps involved in determining the
31 set of parameters α , β and γ from the 1-D doping profile.

5 Fig. 34 illustrates, in one embodiment, top and side views of an exemplary
6 substrate to facilitate discussion of the use of region names and cross-section names
7 as access keys for accessing doping profiles.

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DETAILED DESCRIPTION OF THE INVENTION

6 In the following description, numerous specific details are set forth in order to
7 provide a thorough understanding of the present invention. It will be obvious,
8 however, to one skilled in the art, that the present invention may be practiced without
9 some or all of these specific details. In other instances, well known process steps
10 have not been described in detail in order not to unnecessarily obscure the present
11 invention.

12 An invention is described herein that provides a method and system for IC
13 substrate modeling. The substrate modeling includes modeling characteristics (e.g.,
14 electrical or thermal characteristics) of the substrate as well as characteristics at
15 junctions between the substrate and any immediately overlying devices. Through
16 modeling the parasitic effects of a non-ideal substrate, the degradation in ideal
17 operation of a circuit formed on the substrate may be identified. This permits a circuit
18 designer to modify a circuit design such that it is less sensitive to such parasitic
19 effects. Thus, an operational circuit may be fabricated despite the fact that the
20 substrate is a non-ideal medium. Moreover, the likelihood of circuit failure after
21 fabrication may be significantly reduced.

22 According to one embodiment, a method for characterizing the technology
23 that may be used in a particular substrate is disclosed. As described below, the
24 technology may be characterized through the use of multiple substrate doping
25 profiles. Each of the doping profiles represents a possible combination of doping
26 levels that may be present in a given cross-section of the substrate. In addition, the
27 doping profiles are “vertically discretized” to create subdivisions such that each
28 subdivision corresponds to a range of depth within the substrate. The subdivisions
29 may be placed such that a greater number of subdivisions are created where variation
30 in doping level is greatest. In this manner, the number and location of the
31 subdivisions may be selected such that a balance between accuracy and speed is
32 realized.

33 According to another embodiment, noise present in the substrate may be
34 modeled through the use of a doping profile. A vertical “column” in the substrate
35 may be selected through selecting a position at a surface of the substrate. A

5 combination of layers associated with this vertical column may then be obtained from
6 a circuit layout. The doping profile associated with this combination of layers may
7 then be obtained. Since resistance is associated with each doping level, equivalent
8 resistances throughout the column may then be obtained. In this manner, the substrate
9 may be modeled. In addition, the resistance and capacitance present at junctions
10 between the substrate and overlying layers may be obtained and utilized to associate
11 the substrate model with an existing model of the devices and/or interconnects of the
12 circuit.

13 According to yet another embodiment, an integrated circuit substrate is
14 “horizontally discretized” to create partitions across the surface of the substrate. The
15 doping profile corresponding to each partition may then be selected and applied
16 during the substrate modeling. The number and location of the partitions may be
17 selected to promote accuracy as well as efficiency during the modeling process.

18 Referring first to FIG. 1, a surface view of an exemplary integrated circuit
19 substrate in which the present invention may be implemented is illustrated. As
20 shown, the integrated circuit may be a single MOS transistor. However, those of
21 ordinary skill in the art will readily recognize that the present invention may be useful
22 for a variety of substrates as well as an unlimited number of devices. Integrated
23 circuit substrate 102 includes a p-well 104, p-type diffusion region 106, n-type
24 diffusion region 108, and polysilicon 110. In addition, a metal interconnect 112 is
25 shown. A first vertical column designated by position 114 may be obtained.
26 Similarly, a second vertical column designated by position 116 may be obtained. The
27 first vertical column may be associated with a first doping profile and the second
28 vertical column may be associated with a second doping profile. Each of these
29 doping profiles includes varying net doping levels across the depth of the substrate
30 102. The metal interconnect 112 is connected to the p-type diffusion region 106
31 through a contact 118.

32 FIG. 2A is a cross-sectional view along the line a-a' of FIG. 1. Integrated
33 circuit substrate 202 includes n+ diffusion region 204 that forms a part of integrated
34 circuit device 206. In addition, polysilicon layer 208 is formed above dielectric layer
35 210. A heavily doped p+ diffusion region 212 is formed in the integrated circuit
36 substrate 202 which may be made from silicon or other suitable material. As shown,

5 local oxidation of silicon (LOCOS) 214 is formed in the integrated circuit substrate
6 202. Moreover, metal contact 216 connects metal interconnect 218 to the p+
7 diffusion contact region 212. The first column designated by the position 114 of FIG.
8 1 extends across the line b-b'. As shown, a portion of the first column 114 passes
9 through nodes 220 and 222 within the n+ diffusion region 204. However, the n+
10 diffusion region 204 is part of the device 206 and is therefore modeled during device
11 modeling rather than substrate modeling. Similarly, the second column designated by
12 the position 116 of FIG. 1 extends across the line c-c'. A portion of the second
13 column 116 defines the local oxidation 214 bounded by nodes 224 and 226. In
14 addition, p-type well 228 includes the device 206. The bottom of the p-well is shown
15 at node 230.

16 Referring now to FIG. 2B, an exploded view of FIG. 2A is illustrated. The
17 integrated circuit substrate 202 and each interface (230, 232, and 234) between the
18 substrate and layers directly above the substrate may be modeled according to the
19 present invention. As shown, the integrated device 206 is connected resistively 230
20 and capacitively 232 by the n+ diffusion region 204 to the substrate 202. In addition,
21 since the p+ diffusion region 212 is part of the substrate 202, the metal interconnect
22 218 is resistively 234 interfacing with the substrate 202. Accordingly, the entire
23 substrate and substrate interfaces may be modeled utilizing the present invention.

24 A layout view of the more relevant masks used to fabricate the structure
25 depicted in FIG. 1 is illustrated in FIG. 3. Layer 300 includes p-well 302, layer 308
26 includes n+ diffusion region 310, layer 312 includes p+ diffusion region 314, layer
27 316 includes polysilicon 318, layer 320 includes metal line 322, and layer 324
28 includes contact 326. These ordered layers may then be associated with a doping
29 profile. As will be described in further detail herein, a key may be associated with
30 each doping profile to permit a circuit layout such as that illustrated in FIG. 3 to be
31 associated with multiple doping profiles.

32 Each doping profile includes a net doping level obtained across a cross-section
33 of the substrate. Referring next to FIG. 4, a graph illustrating an exemplary doping
34 profile taken along the line b-b' of FIG. 2A according to one embodiment of the
35 invention is presented. As shown, the graph illustrates a net doping level 402 along
36 the y-axis and the depth 404 of the substrate along the y-axis. Thus, the top surface

5 406 of the substrate is designated at the point (0,0) of the graph, while the bottom of
6 the substrate is designated at point 408. In addition, the n+ diffusion region of FIG.
7 2A is bounded by points 410 and 412, which correspond to the net doping level found
8 at nodes 220 and 222 of FIG. 2A. Since this n+ diffusion region is part of the device
9 206 shown in FIG. 2A, this portion is not utilized during the substrate modeling.
10 Additionally, the bottom of the p-well is shown by point 414, which corresponds to
11 the net doping level found at node 230 of FIG. 2A.

12 FIG. 5 similarly illustrates another exemplary doping profile taken along the
13 line c-c' of FIG. 2A according to one embodiment of the invention. In this doping
14 profile 502, the region bounded by the point 406 and point 414, which corresponds to
15 the net doping level at the node 226 of FIG. 2A, includes LOCOS and therefore this
16 region is not included in the substrate modeling. Moreover, as shown, the net doping
17 level is approximately uniform from point 414 down to point 408 near the bottom of
18 the substrate.

19 The doping profiles may be obtained in several ways. By way of example, net
20 doping levels may be obtained through measurement using a tool such as a scanning
21 electron micrograph. As yet another example, conventional simulation tools such as
22 "TSUPREM" available from Avant!, located in Fremont, California and
23 "SSUPREM3" available from Silvaco, located in Santa Clara, California may be used.
24 Since each device element is typically repeated in multiple locations on a substrate of
25 a typical circuit, each doping profile may be employed to represent more than one
26 vertical column in a given circuit. By way of example, a drain or source of a MOS
27 transistor will be repeatedly formed on the substrate. It is not necessary to provide a
28 separate doping profile for each drain or source of these multiple MOS transistors
29 formed on the substrate. Thus, for a typical circuit, approximately ten profiles may be
30 sufficient to model the substrate.

31 Prior to modeling the substrate of a particular circuit, the technology may be
32 characterized. Referring next to FIG. 6A, a flow diagram illustrating a method for
33 characterizing a particular technology which may be used in a circuit layout according
34 to one embodiment of the invention is presented. The method starts at step 600. At
35 step 602, a name for each layer that may be used in a circuit layout is obtained. By
36 way of example, each combination of layers that may be used in a particular

5 technology (e.g., fabrication process) may be obtained. Moreover, each combination
6 of layers may be in an order in relation to a surface of the substrate. Next, at step 604,
7 an integrated circuit substrate is characterized. According to one embodiment, the
8 substrate is characterized through obtaining a substrate doping profile associated with
9 each possible ordered combination of layers. The layer names and the substrate
10 doping profiles may be obtained from a process engineer such that a relationship
11 between each possible combination of layers and each one of the substrate doping
12 profiles may be ascertained. Thus, the maximum number of substrate doping profiles
13 is 2^n where n is the number of unique layers that may be used during fabrication in
14 this particular technology. However, various combinations of these layers may not be
15 permissible in the construction of certain devices. Thus, the number of possible
16 combinations of layers and therefore the number of profiles will be less than this
17 maximum number of profiles.

18 In addition to the doping profiles, the characteristics of interfaces between the
19 substrate and overlaying devices or interconnects are obtained at step 606. These
20 characteristics may include electrical characteristics such as capacitance and
21 resistance between the substrate and an overlaying circuit layer. By way of example,
22 the overlaying layer may include interconnect lines as well as devices formed above
23 the substrate. According to one embodiment, the capacitance and resistance between
24 the substrate and a layer in immediate contact with the substrate are obtained. Since
25 layers not in direct contact with the substrate are effectively shielded from the
26 substrate by the layer that is in direct contact with the substrate, the interface with
27 these layers may be effectively ignored. Alternatively, the capacitance and resistance
28 between these shielded layers and the substrate layer may be orders of magnitude less
29 than that between the substrate and the layer in immediate contact with the substrate.
30 Moreover, other characteristics of the interface such as thermal characteristics may be
31 obtained. The characteristics of each interface may similarly be obtained from a
32 process engineer.

33 Since each doping profile includes a large number of data points, it is desirable
34 to “compress” these data points to reduce the number of operations that are performed
35 and therefore increase the speed of the modeling process. Thus, once the doping
36 profiles are obtained, the data points, or values, within each doping profile may be

5 “compressed” at step 608. Each doping profile may be compressed through “vertical
6 discretization.” However, it is imperative that this compression be performed without
7 unduly sacrificing the accuracy of the modeling process. One method for performing
8 the vertical discretization will be described in further detail in FIG. 8A – 8D.

9 Next, at step 610, the ordered combination of layers is associated with the
10 corresponding substrate doping profile. According to one embodiment, a unique key
11 is attached to each discretized doping profile to allow correlation with a layout
12 database during the modeling process. The unique key may be created using the
13 ordered combination of layers that may be present in a vertical column within the
14 substrate. The process is completed at step 612. Once the technology has been
15 characterized, the layout information may be utilized during the substrate modeling.

16 One method for obtaining a binary key to a doping profile as provided in step
17 610 of FIG. 6A is illustrated in FIG. 6B. Since the layers in a vertical column at a
18 given location (x, y) are provided in a specified order, the order of the layers may be
19 used to obtain the binary key. By way of example, each ordered layer may be
20 associated with a binary number. A binary key may therefore be obtained by adding
21 the binary number associated with each layer. As shown, a first layer 614 may be an
22 n-well, a second layer 616 may be an n-type diffusion layer, a third layer 618 may be
23 a p-type diffusion layer, and a fourth layer 620 may be a polysilicon layer. If the first
24 layer 614 is given a value of 1, the second layer 616 is given a value of 2, the third
25 layer 618 is given a value of 4, and the fourth layer 620 is given a value of 8, this
26 particular vertical column of layers has a value of 15, or a binary key of 1111.

27 As yet another example, a doping profile may have a polysilicon layer 620
28 and an n-type diffusion layer 616. As described above, the polysilicon layer 620 may
29 have a value of 8 and the n-type diffusion layer 616 may have a value of 2. Thus, a
30 binary key of 1010 may be created.

31 Horizontal discretization of the circuit may be performed to ascertain each
32 position or area of interest in which the characterized technology is modeled.
33 Horizontal discretization may be performed according to various methods. One
34 method includes creating a global grid across a surface of the integrated circuit
35 substrate. The global grid may be uniform or non-uniform. By way of example, a

5 uniform global grid may be created such that it is aligned to the smallest component
6 in the circuit layout. This global grid may be used where all global elements are
7 approximately identical in size. As shown in FIG. 11A, an exemplary global grid is
8 provided across the surface of the integrated circuit substrate. Global elements 1102
9 are approximately identical in size. A segment from global grid 1104 separates the
10 global elements 1102. By way of example, the size of the global segment 1104 may
11 be provided by the design engineer. As yet another example, the maximum number
12 of global segments may be fixed. Accordingly, the size of the global segments may
13 be determined by the size of the integrated circuit to be modeled divided by the
14 maximum number of global segments. Global node 1106 of the integrated circuit
15 substrate or substrate model connects the two global elements 1102. In addition, local
16 nodes 1108 within the global elements 1102 are shown. A component such as
17 resistance 1110 of the substrate model connects local nodes 1108 to global node 1106.
18 Another method includes creating a local grid within a section of the global grid.

19 One method for creating a local grid includes overgridding. As shown in FIG.
20 11B, during overgridding, one or more local grid segments 1112 may be created
21 within the global elements 1102. As shown, the global segment 1104 that is common
22 to two global elements may be split and additional global nodes 1106 may be
23 introduced. The global nodes 1106 may be placed along one or more of the global
24 segments 1104 such that the global segments are subdivided into portions by the
25 global nodes 1106. These global segment portions may be equal or unequal in length.
26 The addition of n global nodes will create n+1 global segment portions. By way of
27 example, as shown in FIG. 11B, the placement of an additional global node creates
28 two additional global segment portions, resulting in two global nodes and three global
29 segment portions. The local grid of the global element 1102 is refined by adding local
30 grid line 1112 together with local nodes 1108. During overgridding, when a local grid
31 line is added, the line divides the global segment 1104 and the corresponding global
32 element 1102 or portion thereof in two portions. The portions are preferably equal
33 but may also be unequal in dimension. By way of example, when more than one local
34 grid line is added during overgridding, the local grid lines may be spaced evenly. As
35 yet another example, the local grid lines may be spaced unevenly to divide the global
36 element into portions having varying dimensions. This may be useful to provide
37 larger portions in the middle of the global element and smaller portions near the

5 boundary of the global element. The local nodes 1108 are then placed in the middle
6 of each newly created portion of the global element 1102, which may be termed "local
7 grid elements." The local grid segments 1112 increase the number of global nodes
8 1106 connecting two global elements 1102, as shown in FIGS. 11A and 11B. In this
9 manner, the number of global nodes connecting two global elements may be increased
10 when the size of the global segment is large to improve the accuracy of the substrate
11 model.

12 Another method for creating the local grid is to add lines where the density of
13 components (devices and interconnects interfacing with the substrate) is high. As
14 shown in figure 11C, component 1114 is bounded by local grid lines 1116 and
15 additional local nodes 1108. The local nodes 1108 are placed in the middle of the
16 local grid elements, as described above. The global nodes 1106 are connected with
17 the closest local nodes 1108. As a result, the local grid 1116 will be fine where the
18 density of the components 1114 is high. As yet another example, a local grid may not
19 be necessary where a global element contains no components. Thus, the level of
20 resolution may be separately maximized for each global element, therefore enhancing
21 the accuracy as well as the efficiency of the substrate modeling.

22 Once horizontal discretization of the circuit is completed, substrate modeling
23 may be performed for each position or area defined by the horizontal discretization
24 process. FIG. 7 illustrates a method for applying the characterized technology
25 obtained in FIG. 6A to a specific circuit layout according to one embodiment of the
26 invention. The process begins at step 702. At step 704, a position (x, y) of interest on
27 a surface of an integrated circuit substrate is obtained. By way of example, a surface
28 view of a circuit such as that illustrated in FIG. 1 may be provided, allowing a user to
29 select the desired position. Next, a combination of layers defining a vertical column
30 beneath the position may be obtained at step 706. By way of example, this
31 combination of layers may be obtained from a layout database. Next, at step 708, a
32 doping profile associated with the combination of layers may be retrieved. By way of
33 example, the doping profile may be obtained through the use of a binary key
34 associated with the combination of layers, as described above. The doping profile
35 may then be used to aid in the modeling process at step 710. The process is
36 completed at step 712.

5 As described in step 608 of FIG. 6A, each doping profile may be vertically
6 discretized through creating a plurality of subdivisions across the depth of the
7 substrate. Each one of the plurality of subdivisions may be created at a different
8 substrate depth such that the number of subdivisions within a range of substrate depth
9 is inversely proportional to the variation in doping level for one or more doping
10 profiles. Thus, the number of subdivisions within each doping profile is minimized to
11 achieve maximum speed. At the same time, a sufficient number of subdivisions are
12 positioned to provide sufficient accuracy during the modeling process. Accordingly,
13 speed of computation is achieved without sacrificing accuracy of the substrate
14 modeling.

15 One method for vertical discretization includes simultaneously aligning
16 subdivisions for a plurality of doping profiles and is illustrated generally in FIGS. 8A
17 – 8D. FIG. 8A is an exemplary graph superimposing multiple doping profiles which
18 may be present in a substrate such as that illustrated in FIG. 2A. The net doping level
19 is illustrated along the y-axis 802 while the substrate depth is illustrated along the x-
20 axis 804. As shown, a first doping profile 806, a second doping profile 808, and a
21 third doping profile 810 are shown. Each level of doping translates into a resistance
22 that is used to provide a substrate model or simulation. By way of example, lower
23 doping levels 812 correspond to a high level of resistance. Similarly, higher doping
24 levels 814 correspond to a low level of resistance. Thus, each doping profile has a
25 corresponding resistivity profile. The resistivity profile therefore includes a
26 resistance corresponding to the net doping level at each one of the plurality of depths
27 within the integrated circuit substrate. The resistance may be obtained from the net
28 doping levels as provided in "Computer Aided Analysis of Parasitic Substrate
29 Coupling in Mixed Digital-Analog CMOS Integrated Circuits" by Francois Clement,
30 presented at the Electrical Engineering Department of (École Polytechnique Fédérale
31 De Lausanne), 1995. This reference is incorporated herein by reference in its entirety
32 and for all purposes. As shown, the resistance will be approximately uniform for a
33 given doping profile as the substrate depth 804 increases. As previously described,
34 each doping profile may contain thousands of points. Thus, it would be desirable to
35 minimize the number of points utilized through the creation of subdivisions at
36 selected depths in the substrate. Since it is preferable to create subdivisions at
37 equivalent substrate depths for each of the doping profiles, it is desirable to ascertain

5 optimum substrate depths at which to place subdivisions for all doping profiles for a
6 given substrate.

7 Since resistivity rather than net doping level is used during substrate
8 modeling, one method for positioning subdivisions for selected doping profiles is
9 through determining the amount of variation of resistivity with respect to the substrate
10 depth. This may be accomplished through ascertaining the slope of each resistivity
11 profile. Since it is irrelevant whether the resistivity is increasing or decreasing, the
12 absolute value of the slope may be obtained. FIG. 8B is an exemplary graph
13 illustrating the absolute values of the slopes of the resistivity profiles of FIG. 8A.
14 Those of ordinary skill in the art will readily recognize that the slope of each
15 resistivity profile may be obtained through calculating the derivative of the resistivity
16 profile curves illustrated in FIG. 8A. Thus, the absolute value of the slope is shown
17 along the y-axis 816 and the substrate depth is shown along the x-axis 804. As
18 shown, the absolute value of the slopes, or derivatives, of the first doping profile 818,
19 the second doping profile 820, and the third doping profile 822 are illustrated.

20 Once the resistivity variation is obtained for each of the profiles, these
21 variations may be combined to obtain an overall variation in the resistivity for
22 multiple doping profiles. FIG. 8C is an exemplary graph illustrating the sum of the
23 curves illustrated in FIG. 8B. As shown, the y-axis represents the sum of the
24 resistivity profile derivatives associated with multiple doping profiles 824 across the
25 depth of the substrate, represented by the x-axis 804. Thus, the sum of the absolute
26 values for multiple resistivity profile derivatives is obtained to yield the overall
27 variation 826 in the resistivity.

28 Through integrating the curve illustrated in FIG. 8C representing the overall
29 variation in the resistivity, it is possible to obtain the area under the curve representing
30 this overall variation. FIG. 8D is an exemplary graph illustrating the integrated sum
31 828 along the y-axis vs. the depth of the substrate along the x-axis 804. As shown, at
32 a maximum substrate depth 830, the resistance will be approximately uniform for a
33 given doping profile. Where there is a large variation in the resistance, a greater
34 number of subdivisions is desirable. Thus, since the variation is greatest close to the
35 surface 832 of the substrate, shown at the origin (0, 0), a greater number of
36 subdivisions along the substrate depth 804 may be created.

5 In order to appropriately place subdivisions along the x-axis, a number of
6 subdivisions desired may be obtained. By way of example, a processing engineer
7 may specify a desired number of subdivisions that may be used across all doping
8 profiles for a particular substrate. Thus, the maximum height 844 of the curve 834
9 may be obtained and divided by the desired number of subdivisions. In this manner,
10 the allowed variation for each vertical subdivision may be obtained. The number of
11 subdivisions are then superimposed on the y-axis and dropped down to the x-axis at
12 the point of intersection with the curve 834 to create subdivision boundaries 836, 838,
13 840. As shown, boundaries 842 may be placed along the y-axis such that the
14 boundaries 842 are evenly spaced along the y-axis. The boundaries along the y-axis
15 are then correlated with the curve 834 at points of intersection to create the
16 subdivision boundaries 836, 838, 840 along the x-axis, representing the depth of the
17 substrate. As shown, each subdivision created along the x-axis intercepts the curve
18 834 as well as the corresponding boundary 842 created along the y-axis. Thus, each
19 subdivision bounded by the subdivision boundaries (e.g., boundaries 836, 838, and
20 840) will correspond to a different resistance. Moreover, as shown, the subdivisions
21 bounded by the boundaries 836, 838, 840 along the depth of the substrate will be
22 unevenly spaced. Accordingly, where there is less change in the doping level, there
23 will be less subdivisions along the depth.

24 Other methods for positioning subdivisions for multiple profiles may be
25 utilized. Since the devices are fabricated at the substrate surface, there is a greater
26 variation in doping level in close proximity to the substrate surface. Because a greater
27 accuracy might be desired closer to the surface than in the depth of the substrate, it
28 may be desirable to create a greater number of subdivisions in this region to maintain
29 a high degree of accuracy during subsequent substrate modeling. Hence, the spacing
30 between the boundaries (e.g., 836, 838, 840) may be decreased in proximity to the
31 substrate surface 832 or increased along the depth of the substrate.

32 In order to provide greater accuracy close to the substrate surface, a spacing
33 ratio may be applied to split the total net doping variation 844 along the depth of the
34 substrate. The spacing ratio may be a constant value which may be multiplied by the
35 width of a subdivision. By way of example, binary values 1, 2, 4, etc. may be utilized
36 as multiplication factors for the width of the subdivisions as the distance from the

5 surface of the substrate increases. Alternatively, the spacing between the boundaries
6 842 may be increased closer to the height of the curve 844. For example, using a
7 multiplication factor of 2 will lead to a net profile variation for one subdivision twice
8 as large as the variation of the previous subdivision. Accordingly, various methods
9 may be applied to adjust the width of each subdivision.

10 As described above, the doping level at a given substrate depth corresponds to
11 a resistance. Thus, each partition within a given doping profile corresponds to a
12 particular resistance that exists within a range of the substrate depth. FIG. 9 is an
13 exemplary block diagram illustrating one method for using a doping profile to aid in
14 substrate modeling 710 shown in FIG. 7. As shown, horizontal discretization may be
15 performed on the substrate 900 to create a plurality of surface area subdivisions. The
16 area 902, or position, of interest on the substrate 900 is then selected. The
17 combination of layers for vertical column 904 defined by that position is then
18 obtained from a layout database. The doping profile, represented by curve 914,
19 corresponding to this combination of layers may then be obtained using a key. The
20 doping profile 914 may then be used to ascertain the equivalent resistance 906
21 associated with each particular block 908 within the vertical column 904 associated
22 with the selected area 902. In this manner, the equivalent resistance throughout each
23 vertical column through the selected area 902, or "slice", within the substrate may be
24 obtained. By way of example, the equivalent resistance can be computed using the
25 algebraic average of the net doping values through a subdivision.

26 As shown in FIG. 9, an equivalent electrical node 910 may be identified for
27 each block 912 within the substrate 900. An equivalent resistance associated with
28 each cube defining the vertical column may therefore be obtained. The equivalent
29 resistance will vary throughout the substrate due to the fabrication process and may be
30 represented by an equivalent horizontal resistance 1012 and an equivalent vertical
31 resistance 1014. In addition, the equivalent resistance will depend in part upon the
32 selection of vertical columns in the substrate through horizontal discretization as well
33 as the positioning of subdivisions in the doping profiles through vertical
34 discretization.

35 FIG. 10 is an exemplary diagram illustrating a method for determining
36 equivalent resistances using a doping profile according to an embodiment of the

5 invention. The accuracy of the substrate model can be improved by distinguishing
6 currents that flow horizontally from currents flowing vertically within a block 1002.
7 After the vertical discretization process, the net doping level within a block will
8 change as a function of the vertical position. As illustrated in FIG. 10, the block 1002
9 is characterized by a discrete number of net doping values 1004 corresponding to a
10 doping profile. Each doping value 1004 further corresponds to a resistance value
11 1006. Each resistance 1006 is seen in parallel by a lateral current 1008 and in series
12 by a vertical current 1010. Thus, the equivalent vertical resistance 1012 may be
13 defined by the sum of the resistances 1006 in the block 1002. Correspondingly, the
14 horizontal equivalent resistance 1014 may be defined by $1/(\Sigma(1/R))$ for the
15 resistances 1006.

16 Once the equivalent resistance is ascertained for each subdivision and block
17 within the substrate, these values may be used to model the noise in the substrate. By
18 way of example, a resistive matrix may be created that includes the equivalent
19 resistance at each node within the substrate. Thus, the resistance and the capacitance
20 at the junction between the substrate and the overlying layer may be combined with
21 the equivalent resistance at each node within the substrate. Using these values, a
22 netlist may be created according to a conventional process. In this manner, RC
23 substrate modeling may be performed.

24 In accordance with one aspect of the present invention, it is found that when
25 the number of devices on the substrate increases, the aforementioned surface or
26 horizontal gridding scheme requires a large number of computations to appropriately
27 model such a high component count, high density substrate. If an engineer needs to
28 add or remove components (such as when “what-if” modeling is performed), the large
29 number of computations would be a disadvantage due to the time delay involved in
30 performing the large number of computations. Accordingly, it would be desirable to
31 employ a surface gridding technique which requires fewer computations to model a
32 given substrate.

33 In accordance with one aspect of the present invention, the substrate is initially
34 initialized into a predefined set of local partitions and gridded into default divisions or
35 grids. If the introduced component overlaps an existing grid of a local partition, that
36 local partition is checked to see whether further partitioning is appropriate. The

5 introduction of a component adds local grid segments, which creates additional
6 divisions out of the existing division or grid. If the additional local grid segments
7 (which arise due to the introduction of a new component) cause the local partition to
8 be subdivided into an unduly large number of divisions (i.e., larger than a specified
9 maximum per local partition), that existing local partition is turned into a global
10 partition containing new local partitions (according to the GridGlobalDivision
11 parameter of the corresponding level). The creation of one additional level of
12 partitioning has the effect of reducing the size of the resultant local partitions, which
13 in turn reduces the number of divisions therein. In other words, since the newly
14 created local partitions are smaller than the old local partition (which was turned into
15 a global partition upon partitioning), there would be fewer divisions per resultant local
16 partition. The new local partitions are checked again to see whether each of them has
17 fewer than the maximum number of allowable divisions therein. If any resultant local
18 partition is found to contain more than the maximum number of allowable divisions
19 therein, that resultant local partition is again turned into a global partition, which
20 further reduces the size of the resultant local partitions. The process recursively
21 continues until no local partition has therein more than the maximum number of
22 allowable divisions or the inserted object is in a global partition that is already at the
23 maximum level (level 2 in our example because GridMaxDepth = 3 leads to 3 levels:
24 level 0, level 1 and level 2).

25 Conversely, when a component is removed, the local grid segments associated
26 therewith are removed from the local partition affected. At that point, the next higher
27 up level of partition (i.e., the immediate higher up global partition) is checked to see
28 whether the number of divisions therein is fewer than the maximum number of
29 allowable divisions. If the next higher up level of partition has fewer than the
30 maximum number of allowable divisions due to the removal of the local grid
31 segments (which were removed because of the removal of the component),
32 simplification is performed since the local partitions are no longer needed for accurate
33 surface modeling. The process recursively continues until no additional
34 simplification is possible, i.e., any additional simplification would cause a local
35 partition to have more than the maximum number of allowable divisions.

5 To facilitate further understanding of this aspect of the present invention, Figs.
6 12A-12F depict a substrate 1202 and the partitioning process that occurs when two
7 objects are inserted in sequence. In Fig. 12A, substrate 1202 is initialized by being
8 partitioned into six top level local partitions A, B, C, D, E, and F. These initial local
9 partitions are generally chosen in accordance with a predefined set of initialization
10 parameters. In the example of Fig. 12 A, the predefined set of grid initialization
11 parameter may, for example, be employed to divide the substrate into a matrix of 3X3
12 (in accordance with parameter GridGlobalDivision0 of Table 1 below). Preferably,
13 however, the ratio is adjusted so that the resulting partitions are quasi-square. In the
14 case of Fig. 12A, since one side of the substrate is smaller than the other, the ratio
15 between the two sides suggests that a 3X2 partitioning scheme would yield quasi-
16 square partitions. Thus, at the top level (level 0), the substrate is divided into a matrix
17 of 3X2.

18 Thereafter, default divisions are formed in each of the local partitions A-F.
19 The default divisions are created responsive to two parameters: OverGriddingFactor
20 and OverGriddingResolution. These factors, which may be user-supplied or may be
21 predefined, indicate how many lines (OverGriddingFactor) are to be created for each
22 resolution (OverGriddingResolution). An example may be OverGriddingFactor = 1
23 and OverGriddingResolution =100 microns, in which case one division is created for
24 each 100 microns.

25 Additionally, the creation of the default divisions may be constrained such that
26 the number of default local grid elements be no greater than the global grid segments
27 of an inferior level if this local partition has to be turned into a global partition at a
28 later time. In the current example, the local partition of level 0 (Fig. 12A) cannot
29 contain more than 1 default local grid segment since the global partition of level 1 is
30 2X2 (as specified by the parameter GridGlobalDivision1 of Table 1 below).

31 The resultant divisions or grids are illustrated in the example of Fig. 12B.
32 Note that in Fig. 12B, each of partitions A, B, C, D, E, and F are still local partitions
33 at this point.

34 Thereafter, components may be inserted in sequence, preferably one-by-one,
35 and each local partition impacted by the insertion (i.e., overlaps at least partially with

5 the component added) is checked to see if any of its existing grid now has a greater
6 than acceptable number of allowable divisions (which is predefined by a variable
7 GridMaxDivisions in the preferred embodiment). For the remainder of the example
8 herein, GridMaxDivisions is set to 4 in order to work through the example.

9 In Fig. 12C, the insertion of object M causes local grid segments 1210, 1212,
10 and 1214 to be added to local partition D. No other partition is affected since object
11 M does not overlap any other local partition. Note that these local grid segments end
12 at the border of the affected local partition, i.e., local grid segments 1210, 1212, 1214
13 terminate at the border of local partition D. At this point, the maximum number of
14 divisions of local partition D does not exceed GridMaxDivisions or 4. In fact, in the
15 Y direction in Fig. 12C, there are 4 divisions (limited by local partition boundaries
16 1260 and 1262, and local grid segments 1214, 1212 and 1213) within local partition
17 D. In the X direction, there are only 3 divisions (limited by local partition boundaries
18 1264 and 1266, and local grid segments 1210 and 1211).

19 In Fig. 12D, an object N is inserted into the substrate. Upon insertion, it is
20 seen that object N intersects two current local partitions: local partition B and local
21 partition D. Initially, the addition of object N would have introduced additional local
22 grid segments 1216, 1218, and 1220 into existing local partition D. Note that since
23 local partition D is still a local partition, the additional local grid elements terminate at
24 its border as shown in Fig. 12D. More significantly, and as seen in Fig. 12D, the
25 introduction of local grid segments 1216 and 1218 would increase the number of
26 divisions in local partition D to over 4. In fact, it is seen that 6 divisions are created in
27 the Y direction (referenced by numbers 1230, 1232, 1234, 1236, 1238 and 1239 in
28 Fig. 12C). Since this is larger than the acceptable number of allowable division
29 (GridMaxDivision, which is 4 in the current example), the local partition D is turned
30 into a global partition (of level 1) and splitted into local partitions (2x2 according to
31 GridGlobalDivision1 parameters that are equal to 2): D1, D2, D3 and D4 as seen in
32 Fig. 12E.

33 Furthermore, in keeping with the rule that local grid segments terminate at the
34 border of the respective local partition, the portions of local grid segments 1212 and
35 1214 that exist to the left of line 1211 in Fig. 12D are removed from Fig. 12E.

5 In Fig. 12F, the new object N is reintroduced into the local partitions D1, D2,
6 D3, and D4 of newly created global partition D. Note that the resultant local
7 partitions are now smaller (each of local partitions D1, D2, D3, and D4 is roughly $\frac{1}{4}$
8 the size of the original local partition D in the example). Equally important is the fact
9 that local grid segments introduced by the addition of object N now terminate at the
10 new local partition borders. In other words, they now terminate at lines 1250 and
11 1252, which are the lines separating new local partitions D1, D2, D3, and D4. As
12 such, local grid segments 1216 and 1218 seen earlier in Fig. 12D do not protrude into
13 local partition D4 of Fig. 12F. Thus, the number of divisions in partition D4 is now 3
14 (shown by reference numbers 1260, 1262, and 1264 in Fig. 12F). Effectively, the
15 additional partitioning of the original local partition D into four local partitions D1,
16 D2, D3, and D4 reduces the number of divisions in each of the local partitions down
17 below the acceptable number of allowable division (GridMaxDivision, which is 4 in
18 the current example).

19 A quick check of Fig. 12F shows that none of the other newly created
20 local partitions have more than 4 divisions in either the X or Y direction. Likewise,
21 the addition of local grid segments 1216 and 1218 (as well as 1270) to existing local
22 partition A does not result in having more than the acceptable number of allowable
23 divisions (GridMaxDivision, which is 4 in the current example). As such, no
24 additional partitioning of local partition A is necessary.

25 In accordance with one aspect of the present invention, the aforementioned
26 surface gridding scheme can be implemented using a recursive algorithm. Figs. 13
27 and 14 show, in one embodiment, the steps taken in initializing a substrate and
28 implementing the inventive surface gridding scheme while inserting an object. In step
29 1302, grid parameters are first obtained. As mentioned, these grid parameters may be
30 obtained from the user or may be predefined. Table 1 illustrates some exemplary
31 parameters.

Name	Value
GridMaxDepth	3
GridGlobalDivision0	3
GridGlobalDivision1	2
GridGlobalDivision2	2
OverGriddingFactor	1
OverGriddingResolution	100 microns
GridMaxDivision	4

Table 1.

8 The GridMaxDepth parameter specifies the maximum number of levels that
 9 the substrate may have. As an example, a local partition is typically turned into a
 10 global partition if the local partition has more divisions than GridMaxDivision.
 11 However, even if a local partition has more divisions than GridMaxDivision, that
 12 local partition will not be turned into a global partition if there are already as many
 13 levels as specified by the parameter GridMaxDepth.

14 Since GridMaxDepth = 3 in this example, the global division at various levels
 15 of depths are provided (e.g., 3, 2, and 2 for GridGlobalDivision0,
 16 GridGlobalDivision1, GridGlobalDivision2, respectively). The GridGlobalDivision
 17 parameter at each level relates to the default number of local partitions that is formed
 18 out of the global partition at that level. As an example, in Fig. 12B, the global
 19 partition is at level 0. In this case, the GridGlobalDivision0 is 3 per Table 1 and,
 20 therefore, the default partitioning is 3X3 local partitions (but adjusted to a matrix 3X2
 21 therein to make the local partitions quasi-square). As another example, in Fig. 12F,

5 the global partition D is at level 1. In this case, the GridGlobalDivision1 is 2 per
6 Table 1 and, therefore, the default partitioning is 2X2 local partitions (i.e., D1, D2,
7 D3, and D4 therein). As a further example, if any of the local partitions D1-D4 is
8 turned into a global partition, that resultant global partition (now at level 2) will have
9 a default partitioning of 2X2 local partitions since GridGlobalDivision2 is 2 per Table
10 1.

11 OverGriddingFactor and OverGriddingResolution, as mentioned earlier, are
12 parameters which determine how a particular local partition may be divided during
13 the initialization stage. In this example, it is specified that a division be provided for
14 every 100 microns. As mentioned, the creation of the default divisions may be
15 constrained such that the number of default local grid elements be no greater than the
16 global grid segments of an inferior level if this local partition has to be turned into a
17 global partition at a later time. In the current example, each local partition in the
18 global partition of level 0 (Fig. 12B) cannot contain more than 1 default local grid
19 segment in either the X or Y direction since the global partition of level 1 is 2X2 (as
20 specified by the parameter GridGlobalDivision1 of Table 1 below).

21 In step 1304, the substrate is initialized at the top level 0. In this step, the
22 appropriate matrix parameters for initially partitioning of the substrate into local
23 partitions such that they are quasi-square are also computed. In step 1306, the default
24 level 0 is created in accordance with the matrix parameters derived in step 1304, such
25 as 3X2 in the present example. The resultant local partitions are shown in Fig. 12A.

26 In step 1308, the default divisions for the local partitions in the global
27 partition of level 0 are created responsive to two OverGridding parameters:
28 OverGriddingFactor and OverGriddingResolution in Table 1, as well as the
29 constraints discussed earlier. The resultant local partitions and divisions are shown in
30 Fig. 12B in which the dotted lines represent the initial overgridding to create the
31 default divisions. The substrate with default level 0 and the default divisions in each
32 local partition is shown in Fig. 12B.

33 In step 1310, the objects are then inserted or removed, and the gridding
34 scheme adjusted accordingly to properly model the surface of the substrate. The
35 process can continue until the modeler is finished (as indicated by arrow 1312).

5 Fig. 14 illustrates, in accordance with one embodiment of the present
6 invention, the steps employed in inserting an object into the substrate (step 1310 of
7 Fig. 13). In general, Fig. 14 is a recursive technique, which steps through each local
8 partition to check 1) which local partition overlaps the newly inserted object; 2) if a
9 local partition overlaps a newly inserted object, whether the introduction of local
10 gridding segments would cause the number of divisions to be greater than
11 GridMaxDivision; and 3) if the answer to question 2 is yes, that local partition is
12 promoted to a global partition, and splitted into local partitions, and the technique
13 recursively goes through the new local partitions to perform steps 1, 2, and 3 for the
14 new local partitions. If all local partitions at a given level do not require further
15 partitioning, the technique pops up one level to continue checking the local partitions
16 at a higher level. The process continues until it is satisfied that no local partition has a
17 greater number of divisions than GridMaxDivision.

18 The recursive technique of Fig. 14 is best understood in connection
19 with Figs. 12A-F. In step 1402, an object O is inserted in substrate G (that is also
20 Global Grid partition of level 0) at the predefined location for insertion (which is
21 provided by the modeler). Initially, object O represents object M of Fig. 12C. At this
22 point, the surface gridding scheme has not been adjusted, if necessary, to
23 accommodate the insertion of the new object.

24 In step 1404, the temporary variable P is set to be the first local partition of G.
25 In Fig. 12C, P = A. In step 1406, it is ascertained whether the newly inserted object O
26 intersects P (which is A at this point). With reference to Fig. 12C, the answer is a
27 negative, and the method proceeds to step 1408 wherein P is set to be the next local
28 partition. Thus, P now equals B, and the method loops back to step 1406 since there
29 are more local partitions to check.

30 The test in step 1406 again results in a negative answer (since object O does
31 not overlap local partition B) and the method proceeds to step 1408 to set P equal to
32 the next partition, which is C. The method loops back to step 1406, obtains a negative
33 answer again (since object O does not intersect C either), and proceeds to step 1408 to
34 set P equal to the next local partition, which is D.

5 The test in step 1406 yields a positive answer this time (since object O
6 overlaps local partition D), and the method proceeds to step 1420 to ascertain whether
7 the current P (which is partition D) is a global partition. Since local partition D is not
8 a global partition at this point, the method proceeds to step 1422 to ascertain whether
9 the insertion of object O into local partition D would cause it to have more divisions
10 than GridMaxDivision. As can be seen in Fig. 12C, the insertion of object O into
11 local partition D causes local grid segments 1210, 1212, and 1214 to be created.
12 However, the number of divisions is smaller than GridMaxDivision. Accordingly, the
13 method proceeds to step 1424 wherein the local partition D (i.e., the local partition
14 currently represented by P) is divided into divisions in accordance with the insertion
15 of object O, with no additional partitioning required.

16 Thereafter, the method proceeds to step 1408 wherein it steps through the
17 remaining local partitions E and F and checks for overlap with the newly inserted
18 object O. Since the answer is negative each time, the method ends when there is no
19 more local partition to check (step 1408 and P already equals to F so that there is no
20 more local partition to set to P). At step 1430, the object O is said to be successfully
21 inserted into the substrate and the surface gridding properly modeled with the new
22 divisions. With reference to Fig. 12C, object M has been successfully inserted and
23 the new surface gridding scheme properly established.

24 The operation of the recursive technique of Fig. 14 may be illustrated again to
25 further understanding with reference to the subsequent insertion of object N. In Fig.
26 12D, object N is inserted into the existing gridding scheme of Fig. 12C (step 1402).
27 In this round, object N is represented by object O in the steps of Fig. 14.

28 In step 1404, P is now local partition A. The test in step 1406 is negative, and
29 P is set to local partition B in step 1408. With P = local partition B, the test in step
30 1406 yields a positive answer (since the new object N intersects local partition B),
31 which causes the method to proceed to step 1420. Since P (local partition B at this
32 point) is not a global partition, the method proceeds to step 1422 to ascertain whether
33 the insertion of object O (object N in this round) into local partition B wouldn't cause
34 local partition B to have more divisions than GridMaxDivision. As can be seen in
35 Fig. 12D, the insertion of object O into local partition B causes local grid segments
36 1216, 1218, 1220 and 1240 to be created, of which local grid element 1240 is located

5 in local partition B and a portion of local grid elements 1216 and 1218 are also
6 located in local partition B. However, local partition B does not have more divisions
7 than GridMaxDivision. Accordingly, the method proceeds to step 1424 wherein the
8 local partition B (i.e., the local partition currently represented by P) is divided into
9 divisions in accordance with the insertion of object O, with no additional partitioning
10 required.

11 Once this is performed, P is set to be equal to the next local partition (local
12 partition C) in step 1408, and the test in step 1406 is negative, and P is then set to the
13 next local partition again (local partition D) in step 1408. The next test in step 1406
14 yields a positive answer since the newly inserted object N (represented by O in this
15 round) also overlaps local partition D. The method then proceeds to step 1420. Note
16 that in the previous round during the insertion of object M, there was no need to
17 partition local partition D, and it remained a local partition until now. Thus, the test
18 in step 1420 yields a negative answer (since local partition D is not a global partition
19 at this point), and the method proceeds to step 1422. In step 1422, it is ascertained
20 that the insertion of object N (represented by object O in this round) does cause local
21 partition D to have more divisions than GridMaxDivision. This can be seen in Fig.
22 12D wherein the addition of local grid segments 1216 and 1218 causes the local
23 partition D to have 6 divisions in the Y direction (represented by reference numbers
24 1230, 1232, 1234, 1236, 1238 and 1239). Thus, the answer to the test in step 1422 is
25 positive, and the method proceeds to step 1442 to create a sublevel in P, essentially
26 promoting the current P (local partition D) to a global partition. Thus, local partition
27 D is splitted into 2x2 local partitions (according to GridGlobalDivisions1). This is
28 done in Fig. 12E.

29 In step 1444, the object O (i.e., object N in this round) is now inserted into the
30 global partition D and more particularly introduced to the local partitions of the newly
31 created global partition D. Recursively speaking, the method pops down one level to
32 level 1 to treat the global partition D in the same way that it treated the entire
33 substrate at level 0 earlier. The new local partitions D1, D2, D3, and D4 are treated in
34 the same way that the local partitions A, B, C, D, E, and F were treated earlier. At
35 this level 1, the level-1 series of steps starts at step 1404, wherein the temporary
36 variable P(1) is now set to be the first local partition D1. As the level-1 series of steps

5 are discussed, the temporary variable P is given the subscript (1) to distinguish it from
6 the temporary variable P in use to check through the local partitions at level 0 (P
7 equals to D when the recursive method pops down to level 1).

8 With reference to Fig. 12F, as $P(1) = D1$, the test in step 1406 yields a
9 negative answer, causing $P(1)$ to be set to $D2$ in step 1408 next. The next test in step
10 1406 turns out to yield positive answer (since the object N does indeed intersect local
11 partition $D2$), and the method proceeds to step 1420, which yields a negative answer
12 since local partition $D2$ is not a global partition at this point in time. The method then
13 proceeds to step 1422 to ascertain whether the introduction of object N to local
14 partition $D2$ would cause the number of divisions therein to be greater than
15 GridMaxDivision . With reference to Fig. 12F, the answer is negative, which causes
16 local partition $D2$ to be divided according to the insertion of object N therein, and no
17 further partitioning of local partition $D2$ is necessary. $D3$ does not intersect object N,
18 and with $P(1)$ set to $D4$, the test in step 1406 turns out to yield negative answer again
19 (since the object N does not intersect local partition $D4$).

20 After local partition $D4$, there are no more local partitions at level 1 to check,
21 and the method pops out of step 1444 back to level 0 to check the remainder of the
22 local partitions E and F. P is next set to local partition E in step 1408 (it should be
23 recalled that P equals to D right before the recursive technique drops down one level
24 to check local partitions $D1$, $D2$, $D3$, and $D4$ of the newly promoted global partition
25 D). Since neither partition E nor F overlaps the newly introduced object N, the
26 method ends when there are no more local partitions at level 0 to check (i.e., when $P =$
27 F and there are no more local partitions to set P to in step 1408). At step 1430, object
28 N is said to be successfully inserted into the substrate and the new gridding scheme
29 successfully implemented to facilitate surface modeling of the substrate, including the
30 newly inserted objects M and N.

31 Fig. 15 illustrates, in accordance with one embodiment of the present
32 invention, the steps employed in removing an object from the substrate (step 1310 of
33 Fig. 13). In general, Fig. 15 is a recursive technique, which reverses the steps taken
34 when an object is inserted. The steps of Fig. 15 may be better understood with the
35 example of Figs. 16 A - 16C, as discussed below.

5 In step 1502, the object O is removed from substrate G. For the sake of
6 example, object O is equivalent to object N, which was inserted earlier in connection
7 with Figs. 12A-F. In step 1504, the temporary variable P is set to be the first local
8 partition of substrate G. In Fig. 16A, P = A. In step 1506, it is ascertained whether
9 the object to be removed (N) overlaps P (which is local partition A at this point).
10 With reference to Fig. 16A, the answer is negative, and the method proceeds via
11 arrow 1508 to step 1510 wherein P is set to be the next local partition. Thus P now
12 equals local partition B, and the method loops back to step 1506 via arrow 1512 since
13 there are more local partitions to check.

14 The result of the test in step 1506 is positive since object N overlaps P (which
15 is local partition B at this point), and the method proceeds to step 1514 wherein it is
16 ascertained whether P (which is local partition B at this point) is a global partition.
17 The answer to the test of step 1514 is negative (the reader is invited to review Figs.
18 12A-F and the discussions in connection therewith, which explain why B is a local
19 partition), and the method proceeds to step 1516 wherein the divisions (e.g., local grid
20 segments) generated by object N are removed from P (P = local partition B at this
21 point). The result of such removal is shown in Fig. 16B.

22 Thereafter, the method proceeds to step 1510 wherein P is set to be the next
23 local partition. Thus P is now equal to local partition C, and the method proceeds
24 back to step 1506 (via arrow 1512) to ascertain whether the object to be removed, N,
25 overlaps the new P (i.e., local partition C). With reference to Fig. 16A, the answer is
26 negative, and the method proceeds via arrow 1508 to step 1510 wherein P is set to be
27 the next local partition. Thus P now equals D, and the method loops back to step
28 1512 since there are more local partitions to check.

29 The result of the test in step 1506 is positive since object N overlaps P (which
30 is D at this point), and the method proceeds to step 1514 wherein it is ascertained
31 whether P (which is D at this point) is a global partition. The answer to the test of
32 step 1514 is positive (the reader is invited to review Figs. 12A-F and the discussions
33 in connection therewith, which explains why D is a global partition), and the method
34 proceeds to step 1530 wherein G is set to be the global partition D and the steps of
35 Fig. 15 are recursively performed to remove object N from global partition D.

5 Recursively speaking, the method pops down to level 1 to treat the global
6 partition D in the same way that the entire substrate is treated up to now. The new
7 local partition D1, D2, D3, and D4 are treated in the same way that local partitions A,
8 B, C, D, E, and F are treated up to now. At this level 1, the level-1 series of steps
9 starts at step 1504, wherein the temporary variable P(1) is set to be the first local
10 partition D1. As the level-1 series of steps are discussed, the temporary variable P is
11 given the subscript (1) to distinguish it from the temporary variable P in use to check
12 through the local partitions at level 0 (P equals to global partition D before the
13 recursive method pops down to level 1).

14 As P(1) = D1, the test in step 1506 yields a negative, and the method proceeds
15 via arrow 1508 to step 1510 wherein P(1) is set to be the next local partition. Thus
16 P(1) is now equal local partition D2, and the method loops back to step 1506 via
17 arrow 1512 since there are more local partitions to check.

18 The result of the test in step 1506 is positive since object N overlaps P(1)
19 (which is D2 at this point), and the method proceeds to step 1514 wherein it is
20 ascertained whether P(1) (which is D2 at this point) is a global partition. The answer
21 to the test of step 1514 is negative (the reader is invited to review Figs. 12A-F and the
22 discussions in connection therewith, which explains why D2 is a local partition), and
23 the method proceeds to step 1516 wherein the divisions generated by object N are
24 removed from P(1), i.e., from local partition D2. The result of such removal is shown
25 in Fig. 16C.

26 Thereafter, the method proceeds to step 1510 wherein P(1) is set to be the next
27 local partition. Thus P(1) is now equal D3, and the method loops back to step 1506
28 via arrow 1512 since there are more local partitions to check. In step 1506, it is
29 ascertained that P(1), which is now D3, does not overlap the object N to be removed,
30 and the method proceeds via arrow 1508 to step 1510 wherein P(1) is set to be the
31 next local partition. Thus P is now equal to D4, and the method loops back to step
32 1506 via arrow 1512 since there are more local partitions to check. In step 1506, it is
33 ascertained that P(1), which is now D4, does not overlap the object N to be removed,
34 and the method proceeds via arrow 1508 to step 1510 wherein it is ascertained that
35 there are no more local partitions to check.

5 Thereafter, the method proceeds to step 1532 to ascertain whether
6 simplification of the global partition D at this level can be done after removal of the
7 object N from its local partitions D1-D4. Note that since the recursive steps are
8 operating at level 1, it is ascertained in step 1532 whether the global partition D can
9 be simplified. Simplification, in this context, means demoting the global partition to a
10 local partition and demoting the local partition(s) therein to divisions. This
11 simplification is preferably performed after it is ascertained that the simplification
12 does not cause the resultant local partition (i.e., D) to have more divisions therein than
13 GridMaxDivision. With reference to Fig. 16C, the demotion of global partition D to a
14 local partition does not cause the resultant local partition to have more divisions
15 therein than GridMaxDivision, and thus simplification is permitted. In this case, the
16 method proceeds to step 1534 to simplify.

17 In step 1536, object N is considered successfully removed from global
18 partition D (which, at this point, has been turned into a local partition), and the
19 recursive method pops up to level 0 out of step 1530 to continue checking the
20 remaining local partitions at level 0, i.e., local partitions E and F. P is next set to local
21 partition E in step 1510 (it should be recalled that P equaled to D right before the
22 recursive technique drops down one level to check local partitions D1, D2, D3, and
23 D4 of global partition D). Since neither partition E nor F overlaps the object to be
24 removed, N, the method proceeds to step 1532 ascertain whether simplification on the
25 global partition at this level can be done after removal of the object N. Since we are
26 at level 0, it is ascertained in step 1532 whether the substrate can be simplified. A
27 review of Fig. 16C suggests that this simplification would have resulted in a local
28 partition having more divisions therein than GridMaxDivision. Thus, simplification is
29 not undertaken. Accordingly, the method proceeds to step 1536 via arrow 1542
30 where object N is considered successfully removed from the substrate. The simplified
31 substrate, with D being a local partition, is shown in Fig. 16D.

32 It may be desirable, at times, to more accurately model the substrate by taking
33 into account the voltage-dependent capacitance across certain junctions (such as the
34 well-substrate junction between the well and substrate bulk). Of course, the
35 capacitances may be obtained by direct measurement or obtained from industry data
36 sources and employed in the modeling of the substrate. In some cases, however, such

5 data may not be available and direct measurement may not be possible or economical
6 or yield the desired accuracy.

7 It is known that the formation of a PN junction gives rise to a space-charge
8 region due to impurity ionization and majority carrier diffusion. See, Computer
9 Aided Analysis Of Parasitic Substrate Coupling In Mixed Digital-Analog CMOS
10 Integrated Circuits by Francois Clement (Ecole Polytechnique Federale de Lausanne,
11 Department d'Electricite, These 1449, 1995), which is incorporated herein by
12 reference. In the substrate, those junctions are reverse-biased, (i.e., there is no current
13 flowing through the junction) and they behave like variable capacitors. For such a
14 junction, the capacitance is given by:

15

16
$$C_t = \frac{A\epsilon_s}{X}$$

17

18 Where A is the area of the junction, X is the thickness of the depletion region,
19 and ϵ_s represents the dielectric constant of silicon. As discussed in the reference
20 Semiconductor-Device Electronics by R.M. Warner and B.L. Grung (Orlando: Holt,
21 Rinehart & Winston, Inc. 1991), which is incorporated herein by reference, the width
22 of the space-charge region, X , can be represented as follows:

23

24
$$X = [\alpha'(\Delta\Psi_0 + V_{NP})]^\gamma \quad Eq. 1$$

25

26 Where V_{NP} is the absolute value of the junction reverse bias voltage and $\Delta\Psi_0$
27 is a constant representing the junction built-in voltage.

28

29

30

31

32

33 Where α' , $\Delta\Psi_0$ and γ' are junction capacitance constants depending on the doping
34 profiles:

	α'	$ \Delta\Psi_0 $	γ'
Asymmetric step junction	$\frac{2\varepsilon(N_A + N_D)}{qN_A N_D}$	$\frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2(T)}\right)$	$\frac{1}{2}$
Linear graded junction	$\frac{12\varepsilon}{qa}$	$\frac{2kT}{q} \ln\left(\frac{aX_0}{n_i(T)}\right) = \frac{qaX_0^3}{12\varepsilon}$	$\frac{1}{3}$

7
8 Where N_A is the concentration of acceptors impurities, N_D is the concentration
9 of donors impurities, and a is the slope; $n_i(T)$ is the intrinsic carrier concentration
10 depending on the temperature T expressed in Kelvin degrees.

11

12 Eq. 1 can be rewritten as:

13

14
$$X = (\alpha + \beta V_{NP})^\gamma$$

15

16 where $\alpha = \alpha' \Delta\Psi_0$, $\beta = \alpha'$ and $\gamma = \gamma'$.

17

18 Thus, the thickness of the depletion region (and thus the capacitance across a
19 well-substrate junction C_t) are related to the three parameters α , β and γ . To put it
20 differently, if the three parameters α , β and γ are known, the capacitance across a
21 well-substrate junction C_t can be calculated for a given bias voltage and employed in
22 the model for a particular well-substrate junction. In the discussion below, techniques
23 for calculating the three parameters α , β and γ from the input 2-D and 1-D mesh
24 doping profile are disclosed. The parameters α , β and γ may be calculated for points
25 along the well-substrate interface, preferably for points corresponding to vertical
26 discretizations.

27 Fig. 17 shows, in accordance with one embodiment of the present invention, a
28 technique for computing the three parameters α , β and γ from the input 2-D mesh
29 doping profile. In step 1702, the 2-D mesh doping profile is obtained. Typically, the
30 2-D mesh doping profile is obtained through a tool such as TSUPREM by Avant!
31 Corp. of Fremont, CA. Fig. 18 shows one example of such a 2-D triangular mesh
32 input data. The concentration of impurities is known in each point of the triangles
33 that comprise the mesh obtained by a finite element simulation of the fabrication
34 process. In Fig. 18, the view is that of a vertical cross-section of the substrate. From
35 the 2-D mesh of Fig. 18, the concentration at any arbitrary point (x, y) of the mesh

5 may be obtained by using, for example, an interpolation technique utilizing the data
6 associated with the vertices of its associated triangle.

7 In step 1704, the junction curve is computed. In general, the junction curve
8 represents a series of points in the 2-D mesh input data such that the concentration of
9 impurities at each point of the curve is zero. In other words, the net concentration of
10 impurities, $c_{net}(x,y)$, is zero along the junction curve.

11 In step 1706, the widths of the space charge region, X , is determined, for a
12 series of voltage values, for each point of the junction curve. As discussed, since the
13 capacitance at the well-substrate junction behaves like a variable capacitor,
14 calculations of the space-charge region are preferably performed for a series of
15 voltage values. In one embodiment, the series of voltage values may represent
16 voltage values that the junction is expected to experience during operation. In another
17 embodiment, the series of voltage values represents the range of voltage values from
18 the minimum value that the circuit is expected to experience, incremented by a
19 reasonable value such as 0.1V, 0.25V, 0.5V, or the like, up to the maximum voltage
20 value that the circuit is expected to experience. Generally speaking, about 10 values
21 may be sufficient.

22 In step 1708, the values of the parameters α , β , and γ may then be obtained.

23 In general, the junction curve may be obtained by any technique that extracts
24 from the 2-D mesh input data a series of points where $c_{net}(x,y) = 0$. In one
25 embodiment, an extrapolation coupled with binary-search algorithm is employed to
26 find the junction curve. This algorithm is discussed in connection with Fig. 19 herein
27 below. In this algorithm, a horizontal line is first drawn through the 2-D mesh input
28 plot of Fig. 18 (shown in Fig. 19 as the line d). Along this horizontal line, the point at
29 which $c_{net}(x,y) = 0$ is determined. This is the first point of the junction curve (shown
30 by R_0 in Fig. 19).

31 Thereafter, additional points may be found by iteratively extrapolating to the
32 next point, and from that next point, find the point along the gradient to the curve
33 where $c_{net}(x,y)$ is again equals to zero. By way of example, if R_{n-1} and R_n are on the
34 junction then R_{n+1} can be obtained by extending the segment (R_{n-1}, R_n) :
35

$$X_n = R_n + (R_n - R_{n-1})$$

7 if X_n is not on the junction, we follow the gradient direction which is orthogonal to
 8 $c_{net}(x,y) = 0$ up to a point Y_n which has a different sign from X_n :

9

$$Y_n = X_n - \text{sign}(\text{cnet}(X_n)) \times \text{grad}(\text{cnet}(X_n))$$

11

12 we then use a bipartition (i.e., binary search) method to exactly determine R_{n+1} .

13 Recursively applying this method leads to a set of points that determines the
14 junction.

15 It should be understood that other techniques may also be employed for
16 obtaining the series of points along the junction curve where $c_{net}(x,y) = 0$. In one
17 embodiment, each point along the junction curve preferably corresponds to a vertical
18 discretization discussed above to limit the number of points that need to be computed.

Once the junction curve is obtained, the width of the depletion region is then determined for each point along the junction curve. In general, the width of the depletion region is determined for each bias voltage, and is calculated along a perpendicular line to the junction curve that intersects the junction curve at the point under consideration. Fig. 20 shows three such perpendicular lines for three points on the junction curve.

25 Though the doping profile of the well-substrate junction (N_D-N_A) can be
26 represented by a gaussian function:

27

$$N_D - N_A = N_0 e^{-\frac{x^2}{a}} - N_A$$

30 this representation is not preferred due to many reasons. By way of example, the
 31 resolution of Poisson's equation is quite complex, and such representation requires the
 32 calibration of parameters N_0 and a from the profile. Furthermore, such representation
 33 is not suitable for all profiles.

34 In accordance with one aspect of the present invention, the solution involves
35 approximating the doping profile by a set of linear functions. One of the advantages

5 of this solution is that it is suitable to all doping profiles shapes. The net doping
 6 profile $N_D - N_A(x)$ will then be divided into q subdivisions in the well part and n
 7 subdivisions in the substrate part as shown in Fig. 21.

8 Linear Function Properties. A discussion of linear function properties now follows.

9 Consider a function $f(y)$ defined on the interval $[0, +\infty]$ by a set of linear functions

10 $f_m(y) \forall m \geq 0$:

11

$$12 f(y) = \begin{cases} f_0(y) = b_0(y - y_0) & y_0 \leq y \leq y_1 \\ f_1(y) = b_0(y_1 - y_0) + b_1(y - y_1) & y_1 \leq y \leq y_2 \\ \dots \\ f_m(y) = \sum_{j=1}^m b_{j-1}(y_j - y_{j-1}) + b_m(y - y_m) & y_m \leq y \leq y_{m+1} \end{cases}$$

13

14 The expression $f_m(y) \forall m \geq 0$ can be rewritten as (here b_j s and y_j s have been switched).

15

$$16 f_m(y) = b_m y + \sum_{j=1}^m y_j (b_{j-1} - b_j)$$

17

18 since $y_0 = 0$.

19

20

21 Well Representation. Back to the substrate-well junction, we consider that the net
 22 doping profile is divided into q subdivisions in the well and that the space charge
 23 region spreads to Y_N , such that $y_q < Y_N < y_{q+1}$. Poisson's equation and continuity
 24 equation are the following:

25

26

$$27 \frac{\delta \xi}{\delta y} = \frac{\rho}{\epsilon_s} = \frac{q_e}{\epsilon_s} (N_D - N_A)_y(y) = \frac{q_e}{\epsilon_s} f(y) \quad Eq. 2$$

28

$$29 \Delta \Psi - V_{NP} = \Psi_n(Y_N) - \Psi_p(X_p) \quad Eq. 3$$

30

31 where $(N_D - N_A)_y(y)$ is the value of the carrier concentration at position y in the
 32 well and with

33

34	ξ	electric field
35	ρ	space-charge density
36	ϵ_s	Dielectric constant of silicon (like ϵ_{Si})
37	$\Delta \Psi$	potential variation across the space-charge region
38	Ψ_N	potential in the n-region
39	Y_N	width of the n-type portion of the space-charge region

5	Ψ_p	<i>potential in the p-region</i>
6	X_p	<i>width of the p-type portion of the space-charge region</i>

7
8
9 Poisson's equation The resolution of the Poisson's equation leads to:

10
11
$$\xi_m(y) = \frac{q_e^-}{\varepsilon_s} \left[b_m \frac{y^2}{2} + \sum_{j=1}^m (b_{j-1} - b_j) y_j y + \sum_{j=m}^{q-1} (b_j - b_{j+1}) \frac{y_{j+1}^2}{2} - b_q \frac{Y_N^2}{2} - \sum_{j=1}^q (b_{j-1} - b_j) y_j Y_N \right]$$

12
13 $\xi_m(y)$ electric field for y such that $y_m < y < y_{m+1}$ and $0 \leq m \leq q$

14
15 Continuity equation The expression of $\Psi_n(Y_N)$ is:

16
17
$$\psi_n(Y_N) = \frac{q_e^-}{\varepsilon_s} \left[b_q \frac{Y_N^3}{3} + \sum_{j=1}^q (b_{j-1} - b_j) y_j \frac{Y_N^2}{2} + \sum_{j=0}^q b_j \left(\frac{y_j^3}{6} - \frac{y_{j+1}^3}{6} \right) + b_q \frac{y_{q+1}^3}{6} \right]$$

18
19 Substrate Representation. For the substrate region, $f(x)$ is defined on $[-\infty, 0]$. The
20 space charge region stretches to X_p , $x_{n+1} < X_p < x_n$ and we similarly have:

21
22
$$f(x) = \begin{cases} f_0(x) = a_0(x - x_0) & x_1 \leq x \leq x_0 \\ f_1(x) = a_0(x_1 - x_0) + a_1(x - x_1) & x_2 \leq x \leq x_1 \\ \dots & \\ f_m(x) = \sum_{j=1}^m a_{j-1}(x_j - x_{j-1}) + a_m(x - x_m) & x_{m+1} \leq x \leq x_m \end{cases}$$

23
24 and thus, $f_m(x), \forall m \geq 0$ can be defined by

25
26
$$f_m(x) = a_m x + \sum_{j=1}^m x_j (a_{j-1} - a_j)$$

27
28
$$\xi_m(x) = \frac{q_e^-}{\varepsilon_s} \left[a_m \frac{x^2}{2} + \sum_{j=1}^m (a_{j-1} - a_j) x_j x + \sum_{j=m}^{n-1} (a_j - a_{j+1}) \frac{x_{j+1}^2}{2} - a_n \frac{X_p^2}{2} - \sum_{j=1}^n (a_{j-1} - a_j) x_j X_p \right]$$

29
30
31
32
$$\psi_p(X_p) = \frac{q_e^-}{\varepsilon_s} \left[a_n \frac{X_p^3}{3} + \sum_{j=1}^n (a_{j-1} - a_j) x_j \frac{X_p^2}{2} + \sum_{j=0}^n a_j \left(\frac{x_j^3}{6} - \frac{x_{j+1}^3}{6} \right) + a_n \frac{x_{n+1}^3}{6} \right]$$

33
34
35
36

5 Width of the Space Charge Region. The width W of the space charge region is given
 6 by $W = Y_N - X_p$. To determine X_p and Y_N the following system is solved:

7 $(\xi_m = 0(0))_n = (\xi_m = 0(0))_p$ Eq. 4

8 $\Delta \Psi - V_{NP} = \Psi_n(Y_N) - \Psi_p(X_p)$ Eq. 5

9 with

10
$$\Delta \Psi = \frac{kT}{q_{e^-}} \ln \left(\frac{(N_D - N_A)_y(Y_N)(N_D - N_A)_x(X_p)}{\eta_i^2} \right)$$

11 If we use the notations:

12
$$\begin{aligned} A_1(m) &= \sum_{j=0}^m (a_j - a_{j+1}) \frac{x_{j+1}^2}{2} & B_1(m) &= \sum_{j=0}^m (b_j - b_{j+1}) \frac{y_{j+1}^2}{2} \\ A_2(m) &= \sum_{j=1}^m (a_{j-1} - a_j) x_j & B_2(m) &= \sum_{j=1}^m (b_{j-1} - b_j) y_j \\ A_3(m) &= \sum_{j=0}^m a_j \left(\frac{x_j^3}{6} - \frac{x_{j+1}^3}{6} \right) & B_3(m) &= \sum_{j=0}^m b_j \left(\frac{y_j^3}{6} - \frac{y_{j+1}^3}{6} \right) \end{aligned}$$

13 the equations (4) and (5) are:

14
$$\frac{q_{e^-}}{\varepsilon_s} \left[B_1(q-1) - b_q \frac{Y_N^2}{2} - B_2(q) Y_N \right] = \frac{q_{e^-}}{\varepsilon_s} \left[A_1(n-1) - a_n \frac{X_p^2}{2} - A_2(n) X_p \right] \text{ Eq. 6}$$

15
$$\Delta \Psi - V_{NP} = \Psi_n(Y_N) - \Psi_p(X_p)$$
 Eq. 7

16 where

17
$$\Psi_n(Y_N) = \frac{q_{e^-}}{\varepsilon_s} \left[b_q \frac{Y_N^3}{3} + B_2(q) \frac{Y_N^2}{2} + B_3(q) + b_q \frac{y_{q+1}^3}{6} \right]$$
 Eq. 8

18
$$\Psi_p(X_p) = \frac{q_{e^-}}{\varepsilon_s} \left[a_n \frac{X_p^3}{3} + A_2(n) \frac{X_p^2}{2} + A_3(n) + a_n \frac{x_{n+1}^3}{6} \right]$$
 Eq. 9

19 Resolution of the System. Equation 6 depends on X_p and Y_N . We can express X_p
 20 from Y_N as follows:

5
$$X_p = \frac{-A_2(n) \pm \sqrt{A_2(n)^2 + 2a_n(A_1(n-1) - B_1(q-1) + b_q \frac{Y_N^2}{2} + B_2(q)Y_N)}}{a_n}$$

6

7 but only root (10) will be used for $X_p < 0$:

8

9
$$X_p = \frac{-A_2(n) - \sqrt{A_2(n)^2 + 2a_n(A_1(n-1) - B_1(q-1) + b_q \frac{Y_N^2}{2} + B_2(q)Y_N)}}{a_n} \quad Eq. 10$$

10

11 knowing that $y_{q+1} = Y_N$ and $x_{n+1} = X_p$, we can rewrite equations (8) and (9) into

12

13
$$\Psi_n(Y_N) = \frac{q_e^-}{\varepsilon_s} \left[b_q \frac{Y_N^3}{3} + B_2(q) \frac{Y_N^2}{2} + B_3(q-1) + b_q \frac{y_q^3}{6} \right]$$

14

15
$$\Psi_p(X_p) = \frac{q_e^-}{\varepsilon_s} \left[a_n \frac{X_p^3}{3} + A_2(n) \frac{X_p^2}{2} + A_3(n-1) + a_n \frac{x_n^3}{6} \right]$$

16

17 and try to solve (7) to determine Y_p . Equation (7) will also be noted $F(Y)$ if X_p
18 is replaced by (10).

19 The algorithm that corresponds to the search of X_p and Y_N for each voltage is
20 presented in Fig. 22. Steps 2200-2214 of the algorithm consists of determining $\Delta \Psi$.
21 To do so, the bias voltage value $V_{NP} = 0$ is first employed. In one embodiment, a
22 piece-wise approximation technique is employed. The computation of Y_{N0} and X_{P0}
23 (i.e., the value of Y_N and X_p for $V_{NP} = 0$) involves a loop (steps 2208 and 2210) that
24 approximates these two variables. At the start, $n = 0$ and $q = 0$ (see Fig. 21) and Eqs.
25 2 and 3 are solved to obtain two values for Y_{N0} and X_{P0} . If Y_{N0} is greater than y_{q+1}
26 (resp. X_{P0} less than x_{n+1}) which means that Y_N is out of the approximation interval, Y_{N0}
27 (resp. X_{P0}) is recomputed with a more accurate interval. In other words, some more
28 slope is added to the linear function that approximates $(N_D - N_A)$ in the well part and
29 increment q (resp. n).

30 Once Y_{N0} and X_{P0} are obtained, $\Delta \Psi$ can be calculated (see Eq. 3) since if $V_{NP} =$
31 0,

32

33
$$\Delta \Psi = \Psi_n(Y_{N0}) - \Psi_p(X_{P0})$$

34

5 The value of $\Delta \Psi$ facilitates the calculation of Y_N and X_P for other bias
 6 voltages. These are shown in Fig. 22 as steps 2216-2228.

Example 1

11 Consider that $n = 0, q = 0, a_0 = b_0 = 5e^{+19}$. Then we have from Equation 10:

$$X_p = -\sqrt{\frac{b_0}{a_0}} Y_N$$

15 and from Equation 7:

$$17 \quad \frac{kT}{q_e^-} \ln \left(\frac{(a_0 X_p)(b_0 Y_N)}{\eta_i^2} \right) - \frac{q_e^-}{\varepsilon_s} \left[b_0 \frac{Y_N^3}{3} - a_0 \frac{X_p^3}{3} \right] = 0$$

$$F(Y) = \frac{kT}{q_{e^-}} \ln \left(\frac{b_0 \sqrt{a_0 b_0} Y_N^2}{\eta_i^2} \right) - \frac{q_{e^-}}{\varepsilon_s} \left[\frac{b_0}{3} Y_N^3 \left(1 + \sqrt{\frac{b_0}{a_0}} \right) \right] = 0$$

21 The resolution of this equation with the following constants:

$$\begin{aligned}q_e^- &= 1.6021e^{-19} C \\ \varepsilon_s &= 103.596e^{-14} F/cm \\ \eta_i &= 1.45e^{+10} cm^{-3} \\ \frac{kT}{q_e^-} &= 0.02585\end{aligned}$$

26 leads to $Y_N = 4.94e^{-5} \text{ cm}$ for $V_{NP} = 0$. $\Delta \Psi$ is then equal to 0.622797.

27 Figs. 23, 24, and 25 illustrate the function $F(Y)$ for different bias voltages V_{NP}
 28 (0V, 0.25V, and 0.5V respectively) or this example.

29 The resultant widths of the depletion region for various bias voltages of this
 30 example is set forth in the table shown in Fig. 26.

Example 2

33 For this second example, consider now that $n = 1$, $q = 1$, $a_0 = b_0 = 5e^{+19}$, $a_1 =$
 34 $1e^{+18}$, $b_1 = 0.5e^{+18}$:

$$\begin{aligned}
 5 \quad A_1(0) &= (a_0 - a_1) \frac{x_1^2}{2} & B_1(0) &= (b_0 - b_1) \frac{y_1^2}{2} \\
 A_2(1) &= (a_0 - a_1)x_1 & B_2(1) &= (b_0 - b_1)y_1 \\
 A_3(0) &= a_0 \left(\frac{x_0^3}{6} - \frac{x_1^3}{6} \right) = -a_0 \frac{x_1^3}{6} & B_3(0) &= b_0 \left(\frac{y_0^3}{6} - \frac{y_1^3}{6} \right) = -b_0 \frac{y_1^3}{6}
 \end{aligned}$$

6
7
8

$$9 \quad X_p = \frac{-A_2(1) - \sqrt{A_2(1)^2 + 2a_1 \left(A_1(0) - B_1(0) + b_1 \frac{Y_N^2}{2} + B_2(1)Y_N \right)}}{a_1}$$

10
11

$$12 \quad \Psi_n(Y_N) = \frac{q_{e^-}}{\varepsilon_s} \left[b_1 \frac{Y_N^3}{3} + B_2(1) \frac{Y_N^2}{2} + B_3(0) + b_1 \frac{y_1^3}{6} \right]$$

13

$$14 \quad \Psi_p(X_p) = \frac{q_{e^-}}{\varepsilon_{s2}} \left[a_1 \frac{X_p^3}{3} + A_2(1) \frac{X_p^2}{2} + A_3(0) + a_1 \frac{x_1^3}{6} \right]$$

15

16 and equation 7:

17

$$18 \quad F(Y) = \frac{kT}{q_{e^-}} \ln \left(\frac{(a_1 X_p + (a_0 - a_1)x_1)(b_1 Y_N + (b_0 - b_1)y_1)}{\eta_i^2} \right) - \frac{q_{e^-}}{\varepsilon_s} [\Psi_n(Y_N) - \Psi_p(X_p)] = 0$$

19

20

21 The resultant widths of the depletion region for various bias voltages of this
22 example is set forth in the table shown in Fig. 27.

23 From the widths of the depletion region for various bias voltages, the set of
24 parameters α , β and γ may then be computed. In one embodiment, if a vertical
25 subdivision includes more than one point for which the widths of the depletion
26 regions at various bias voltages have been calculated, an average may be taken so that
27 for each bias voltage level, an average width may be obtained for all the points within
28 the vertical subdivision. Doing so simplifies the modeling subsequently since only
29 one set of values α , β and γ needs to be obtained for that vertical subdivision based on
30 the average value.

31 Computation of Parameters α , β and γ One technique for deriving these
32 parameters α , β and γ is set forth below. It should be noted, however, that other

5 mathematical techniques, other than the preferred technique set forth below, may also
6 be employed to solve for parameters α , β and γ .

7 Consider a function given by a set of pairs $\{(f_i, v_i)\}$, $0 \leq i \leq n$, where $f_i =$
8 $f_{\alpha, \beta, \gamma}(v_i)$. Fig. 28 depicts an exemplary plot of voltages v_i versus the corresponding
9 widths (f_i) . The function $f_{\alpha, \beta, \gamma}(v_i)$ has the following format:

10
11
$$f_i = f_{\alpha, \beta, \gamma}(v_i) = (\alpha + \beta v_i)^\gamma, \forall i, 0 \leq i \leq n$$

12

13 To determine α , β and γ we use a simple method:

14 1. We first express α and β in function of γ for $i = 0$

15
16
$$f_0 = (\alpha + \beta v_0)^\gamma$$

17

18 but $v_0 = 0$, and then

19
20
$$\alpha = e^{\frac{\ln(f_0)}{\gamma}}$$

21

22 we approximate β with the last point of the function ($i = n$):

23
24
$$f_n = (\alpha + \beta v_n)^\gamma$$

25

26
27
$$\beta = \frac{e^{\frac{\ln(f_n)}{\gamma}} - \alpha}{v_n}$$

28

29 2. Given that $\gamma \in \frac{1}{3} \dots \frac{1}{2}$, we iteratively compute α , β and the error function

30
31
$$e(\alpha, \beta, \gamma) = \sum_{i=0}^n (f_i - (\alpha + \beta v_i)^\gamma)^2$$

32 for a set of values of γ in the defined interval and retain the value that minimizes the
33 error function.

34 This method, though very simple, seems to give precise results as shown by
35 the sets of exemplary values presented in the tables of Figs. 29 and 30. Figs. 31 and
36 32 show for each set of values the linear function $\{f_i, v_i\}$ and the corresponding
37 approximated function.

Once the three parameters, α , β , and γ , which characterize the well-substrate junction for a particular point in a vertical discretization, are calculated, these parameters may be stored in the database and employed to more accurately model the substrate at modeling time. By way of example, during modeling, the bias potential for each well may be provided and the specific capacitance that connect nodes of the mesh within the well to nodes of the mesh in the substrate across the well-substrate junction, which specific capacitance is associated with the specified bias potential and the specific vertical discretization, may be determined. If the resistance is very large compared to the capacitance, it may be possible, in one embodiment, to ignore the resistance altogether in modeling the well-substrate junction (of course, whether one wishes to ignore the resistance value depends on the accuracy desired). Since the specific capacitance is calculated in view of the doping concentrations and the bias potential, instead of a static value as in the case when the capacitance is provided as a value used in industry and obtained by measurement of the physical structure, a more accurate 3-D mesh model may be obtained.

Note that although only one junction curve is illustrated to simplify the discussion, the capacitance determination technique of the present invention may also be employed when there are multiple junction curves, e.g., in the case where the process is complex.

In some cases, however, the process engineer can only provide a 1-D description of the doping profiles: each cross-section of the process is then represented by a carrier concentration versus the substrate depth. By way of example, Fig. 8A shows one such example of a 1-D profile.

In this case we apply to each junction a similar algorithm used for a 2-D mesh to compute the depletion region width for each p-n transition inside the vertical doping profile. The result is still a set of parameters α , β and γ . Fig. 33 illustrates the steps involved in determining the set of parameters α , β and γ when only the 1-D doping profile information is available.

To compute the perimeter values C_p between region *Default* and *n-well* from the 1-D carrier concentrations, we assume that the charge distribution as a function of

5 distance is an abrupt or step junction. Between two adjacent subdivisions i and j , the
6 density of space charge on the n and p sides of the step junction will be given by
7 $-qN_{Aij}$ and qN_{Dij} , where N_{Aij} and N_{Dij} stand for the average carrier concentrations of
8 the 1-D default profiles. Then, α , β , γ for perimeter capacitances are given as follows:

9

10 $\gamma_{ij} = \gamma_2$

11

12
$$\alpha_{i,j} = \frac{2\epsilon_0\epsilon_{Si}}{q_{e^-}} x \frac{N_{Aij} + N_{Dij}}{N_{Aij}N_{Dij}} x \frac{kT}{q_{e^-}} \ln\left(\frac{N_{Aij}N_{Dij}}{n_i^2(T)}\right)$$

13

14

15
$$\beta_{i,j} = \frac{2\epsilon_0\epsilon_{Si}}{q_{e^-}} x \frac{N_{Aij} + N_{Dij}}{N_{Aij}N_{Dij}}$$

16

17 where

18

19 ϵ_0 *permittivity of free space (8.86 e^{-14} F/cm)*
20 ϵ_{Si} *dielectric constant of silicon (11.7)*
21 N_{Aij} *concentration of acceptor impurities between subdivisions i and j*
22 N_{Dij} *concentration of donor impurities between subdivisions i and j*
23 k *Boltzmann's constant*
24 T *Temperature in Kelvin*
25 q_{e^-} *magnitude of electronic charge (1.6e $^{-19}$ C)*
26 $n_i(T)$ *intrinsic carrier concentration (dependent on T)*

27

28 Once the three parameters α , β , and γ are obtained, they may be employed to
29 calculate the specific capacitance at that junction in the manner discussed earlier.

30

31 As mentioned earlier, each doping profile is associated with an access key to
32 facilitate correlation with the layers of the layout database. Also as mentioned earlier
33 in connection with Fig. 6B, a binary key, which is formed by adding the binary value
34 associated with each of the ordered layers, may be employed for accessing a specific
35 doping profile in one embodiment.

36 In another embodiment of the present invention, the unique access key
37 may be formed by a combination of a region name and a cross-section name. This
38 access key is created, in part, to render the process of accessing doping profiles more
39 user-friendly to professionals, such as foundry professionals, who are more

5 comfortable working with regions and cross-sections when fabricating devices on a
6 substrate.

7 For the purpose of this portion of the discussion, a region is identified as an
8 area of the substrate in which the number of transitions between p-type material and
9 n-type material within the bulk underlying that area remains the same. Furthermore,
10 the vertical positions of those transitions within the bulk underlying that area also
11 remains the same (within tolerance limits). Different regions have either different
12 numbers of transitions between the p-type material and the n-type material, or
13 different locations for those transitions, or both. For a particular substrate, region
14 specification may come from a variety of sources, including, for example, foundry
15 professionals.

16 One may think of region names as, for example, coarse information, which
17 provides information pertaining to whether an area has no well, a single well, or a
18 triple well, or the like, and how deep are the transitions. A substrate may have any
19 number of regions.

20 Within each region, there may be different structures which one may wish to
21 fabricate. Each structure fabricated in a given region will result in a variation of
22 carrier densities therein. One example of such a structure is a contact. However, a
23 contact may occur in many different regions, and the cross-section associated with a
24 contact may not be unique on its own. For this reason, a combination of the specific
25 region and the specific cross-section is needed for uniqueness, and it is from this
26 combination of both the region name and the cross-section name that the access key is
27 created. In this manner, the cross-section name may be thought as more detailed
28 information which, when used in combination with the coarser information (i.e., the
29 region name) would yield a unique combination suitable for use as an access key.

30 To facilitate further understanding, an example is discussed in connection with
31 Fig. 34 herein. Fig. 34 illustrates, in accordance with one embodiment of the present
32 invention, an exemplary portion of a substrate having default regions 3401 and an n-
33 well region 3402. Note that there are two default regions to both sides of n-well
34 region 3402 since within these two default regions, the number of transitions is the
35 same (i.e., both have zero transition) and the vertical locations of the transitions are

5 the same (i.e., none in this case). For each region, a default cross-section is provided.
6 In the example of Fig. 34, the default cross section for default region 3401 is indicated
7 by a reference number 3404. This default cross-section 3404 represents the cross-
8 section employed with default region 3401 if no specific cross-section is indicated.
9 As another example, the default cross-section for n-well region 3402 is indicated by a
10 reference number 3406. Again, this default cross-section 3406 represents the cross-
11 section employed with n-well region 3402 if no specific cross-section is indicated.
12 Note also that although both cross-sections 3404 and 3406 are default cross-sections,
13 they are different in their doping profiles due to the fact that they occur in different
14 regions.

15 Within default region 3401, a specific cross-section 3403 "contact" is shown.
16 Within n-well region 3402, a specific cross-section 3405 "contact" is also shown.
17 When each of these cross-sections is combined with its respective region (or when
18 each of the default cross-sections is combined with its respective region for that
19 matter), a unique identifier is obtained, which may be used as an access key to a
20 doping profile associated therewith.

21 For some people, the formation of a unique access key from the combination
22 of a region name and a cross-section name may be more intuitive. Instead of having
23 to enter all individual layers in every combination, compute their associated binary
24 values, and use those binary values as unique access keys, the present technique
25 allows one to form a unique access key to a doping profile from fewer constituent
26 parts (e.g., from the region name and cross-section name). This is particularly user-
27 friendly if one already has access to information pertaining to the cross-section name
28 and the region name for each location on the substrate.

29 Furthermore, the use of region names (in combination with cross-section
30 names) to access the doping profiles also clearly identifies the presence of n-type to p-
31 type transitions and yields clues about whether different doping profiles involve
32 different transition depths. In this manner, it is possible to quickly determine whether
33 it is necessary to add junction capacitances in the substrate model. By way of
34 example, a junction capacitance is necessary whenever there is a vertical transition
35 from n-type to p-type material within the structure. By way of another example, when
36 two different regions are placed next to each other there will be at least one lateral n-

5 type to p-type transition that requires the addition of the corresponding junction
6 capacitance in the substrate model. This is an advantage over the binary access key,
7 as can be appreciated by those skilled in the art.

8 The present invention provides numerous advantages. Through utilizing
9 doping profiles, substrate characteristics may be accurately and efficiently modeled.
10 Moreover, through creating vertical subdivisions in these doping profiles, the
11 accuracy and efficiency of this modeling is maximized. Similarly, through creating
12 horizontal subdivisions in an integrated circuit substrate, the doping profiles may be
13 accurately and efficiently utilized during the modeling process.

14 The present invention may generally be implemented on any suitable
15 computer system. The computer system may include any number of processors that
16 may be coupled to memory devices such as a read only memory (ROM) or a random
17 access memory (RAM). In addition, it is contemplated that such a computer system
18 might be connected to a network to receive information from the network or output
19 information to the network.

20 The invention can also be embodied as computer readable code on a computer
21 readable medium. The computer readable medium is any data storage device that can
22 store data which can thereafter be read by a computer system. Examples of the
23 computer readable medium include read-only memory, random-access memory, CD-
24 ROMs, magnetic tape, and optical data storage devices. The computer readable
25 medium can also be distributed over a network between coupled computer systems so
26 that the computer readable code is stored and executed in a distributed fashion.

27 Although illustrative embodiments and applications of this invention are
28 shown and described herein, many variations and modifications are possible which
29 remain within the concept, scope, and spirit of the invention, and these variations
30 would become clear to those of ordinary skill in the art after perusal of this
31 application. For instance, the present invention is described as modeling electrical
32 characteristics of a substrate. However, it should be understood that the invention is
33 not limited to modeling characteristics of this type, but instead would equally apply
34 regardless of the characteristics modeled. Accordingly, the present embodiments are
35 to be considered as illustrative and not restrictive, and the invention is not to be

5 limited to the details given herein, but may be modified within the scope and
6 equivalents of the appended claims.